SC'16 BoF Report : Intel QuickAssist user gathering

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Abstract

In 2015, Intel made a number of experimental systems incorporating Intel QuickAssist technology available. The systems consist of an Intel processor tightly connected to an Altera FPGA via direct package pins.

The Intel QuickAssist user gathering BoF aimed at providing a forum for users of the aforementioned systems, or users of QuickAssist technology, to exchange experiences. The end goal was to build a community for the QuickAssist technology.

The BoF had two prepared presentations and one improvised. The rest of the time of the BoF was used by users to exchange experiences and news. The consensus was that a community should be established and the first steps for that was decided.

1 Introduction

In 2015, Intel made a number of systems available to the research community under the "Heterogeneous Architecture Research Platform" program. Thus, providing a very capable experimental platform for architectural research for high performance computing. Recently, Intel has announced a continuation of the program named the "Hardware Accelerator Research Program".

The purpose of the BoF session was to bring together persons interested in the aforementioned systems, in the Intel QuickAssist as well as persons interested in the use of FPGAs in high performance computing. The platform that Intel has provided is very useful for prototyping high performance

systems as it tightly connects a high-end Altera FPGA with an Intel server processor.

The goal of the BoF session was to attempt to build a user driven community around users of the QuickAssist systems but also FPGAs in general.

2 Outline of activities at the BoF

The BoF had a varying number of attendees of between seven and ten attendees. However, all attendees were active in discussions. The entire length of the BoF was used with most of the time taken up by discussions.

At the start of the BoF the start of the "BoF: Intel QuickAssist User Gathering" slide deck was shown to provide a context for the BoF and structure to the discussions. Given the number of attendees, we did an informal round-table of attendees allowing everyone to speak about their interests. Interests were wide ranging from exascale systems to acceleration of connection level network encryption.

Several attendees asked for more information on Intels experimental systems and a representative from Intel provided answers.

DTU as well as Argonne National Laboratory presented slides on what they are working on. DTUs slides were "Experiences with Intel-Altera HARP / Intel QuickAssist" while ANL reused slides from an prior SC workshop.

The attendees discussed if a community should be build and how. The general conclusion was that a community should be built. This was voiced at the BoF itself but also via mail as well as off-line discussions before and after the BoF.

3 Outcome and next steps

The most operational outcome was that attendees and other users agreed that a community should be built.

Also, a brief strategy to do that was put together as follows. Below some comments on the current status of the strategy have been added.

- An open mailing list is to be created. The mailing list is now created and anyone can subscribe via the following URL: `https://lists.fenixforge.com/mailman/listinfo/fpga-discussion`.

- Bi-monthly regular teleconference are to be held. The first teleconference is expected to be held in January 2017.
- A wiki for technology is to be established so that users can share experiences and technology. The wiki is yet to be established.
- Meetings at major conferences are to be held. At the BoF there was an interest in having a meeting at the next SC. Other major conferences such as HPCA was mentioned. In addition, Argonne National Laboratory volunteered to host a meeting. Location, schedule and scope of the next meeting is to be discussed at the first teleconference.

In all the BoF was a success!