BoF on “Use cases of Reconfigurable Computing Architectures for HPC”

SC16, November 17th, Salt Lake City

Basics

The Birds of a Feather session took place on November 17 between 12:15 and 1:15 pm. Rough number of participants in the audience was 70.

The short intro presentation and the three of the four “feature presentations” are appended to this report. We did ask to have the discussion with the audience after each presentation.

Rainer Schwemmer: Use Cases of Reconfigurable Computing Architectures for HEP

Q: Is the data filtering presented done in real time?

A: Yes – within 10 – 100 µsec, decision is reached whether to read out the full data; this would need ASICs if it weren’t for FPGAs.

David Donofrio: Specialization and Open Source Hardware to Enable Continued Performance Scaling

Q: Is the intermediate representation mentioned an extension of the LLVM IR?

A: No – it is a well-designed IR unrelated to LLVM.

Richard Veitch: Maxeler Presentation (not included here)

Q: None.

Jordà Polo: Scaling Genomics Workloads

Q: Are any preliminary results available?

A: Yes – time take on 16 nodes is approx. 10 hours; time for the FOGA implementation on one node is likewise 10 hours. Our target is to arrive at a runtime of 1 hour on a single FPGA- and NVM-equipped node.

Points addressed

- New domain for HPC, for addressing which kind of problems?
- Share your experience
- What are the gaps
  - Programmability
  - Efficiency
  - New workloads
  - ……..
- What do we need to do as a community?

"Still nothing. You sure this is the best computer we have?"

Speakers

Rainer Schwemmer, CERN

David Donofrio, LBL

Richard Veitch, Maxeler

Jordà Polo, BSC

Specialization and open source hardware to enable continued performance scaling

David Donofrio

Berkeley National Labs

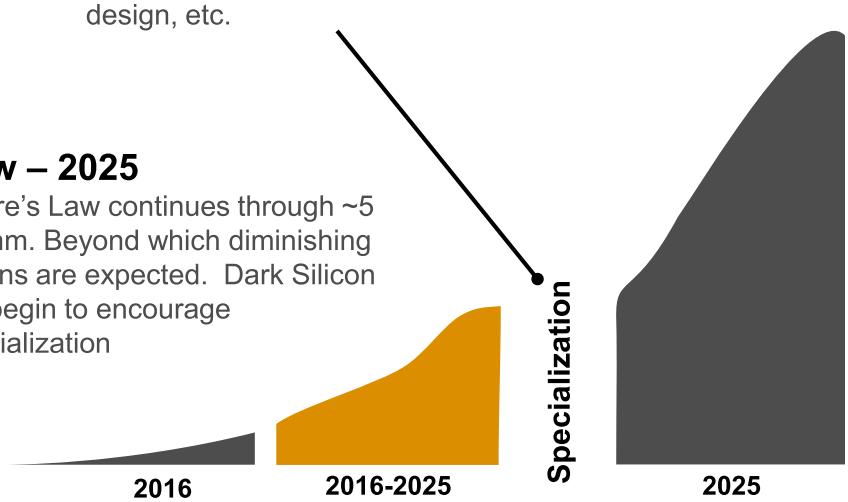
Post Moore Technology Curve

Great *opportunities* exist for innovation through the end of Moore's Law

End of Moore's Law
End of Moore's Law requires a different set of optimizations to continue performance scaling. Opportunities for additional specialization, reconfigurable computing, hardware / software co-design, etc.

Throughout…
Continued increases in parallelism and heterogeneity will require advanced runtimes, programming environments and compiler optimizations in order to take full advantage of these new architectures

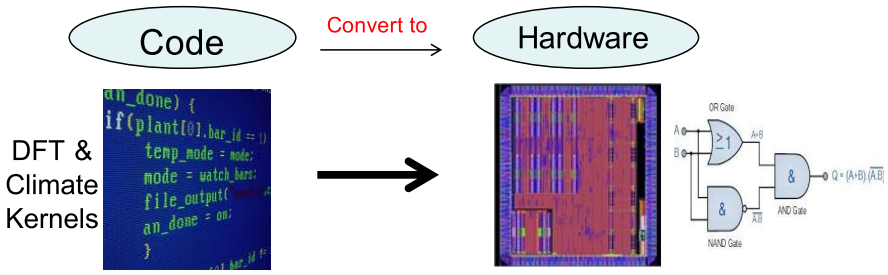
Now – 2025
Moore's Law continues through ~5 or 7nm. Beyond which diminishing returns are expected. Dark Silicon will begin to encourage specialization

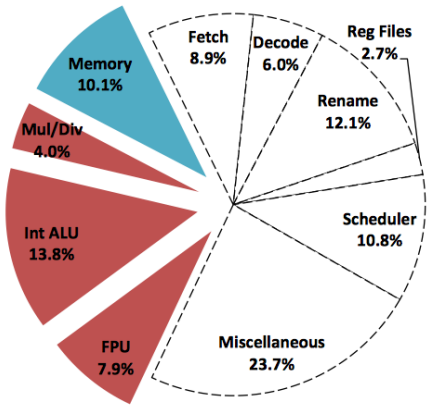


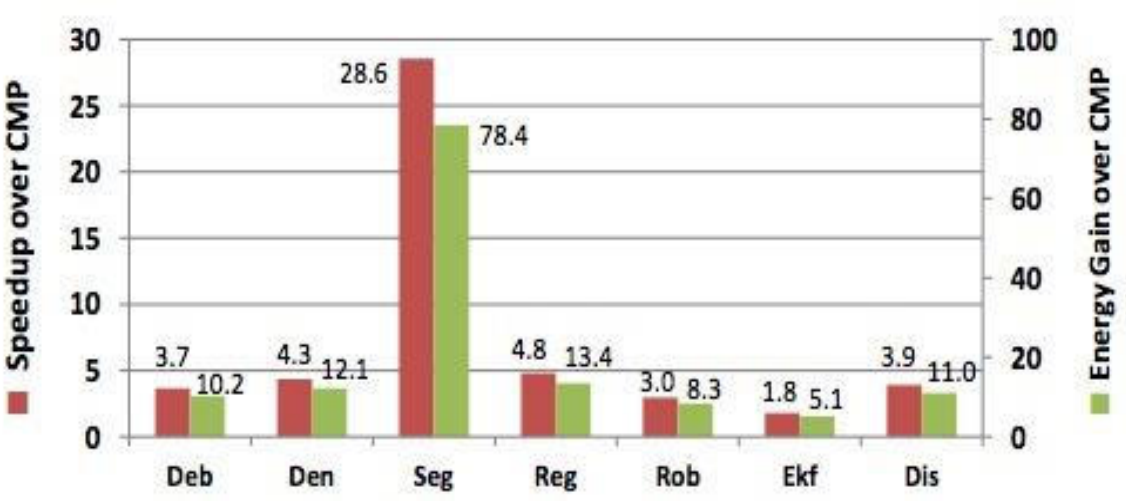
Post Moore Scaling
New materials possibly introduced to allow continued process and performance scaling.

Current architectures are wasteful

How far can we push performance scaling using specialization?



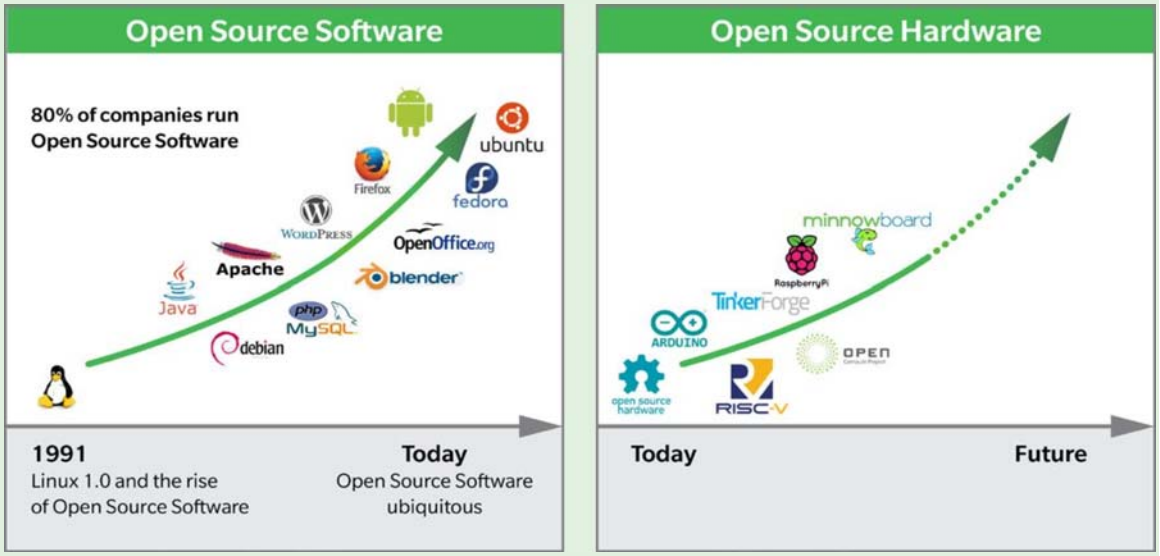




Open Source Hardware

Driving the next wave of innovation

The Rise of Open Source Software: Will Hardware Follow Suit?



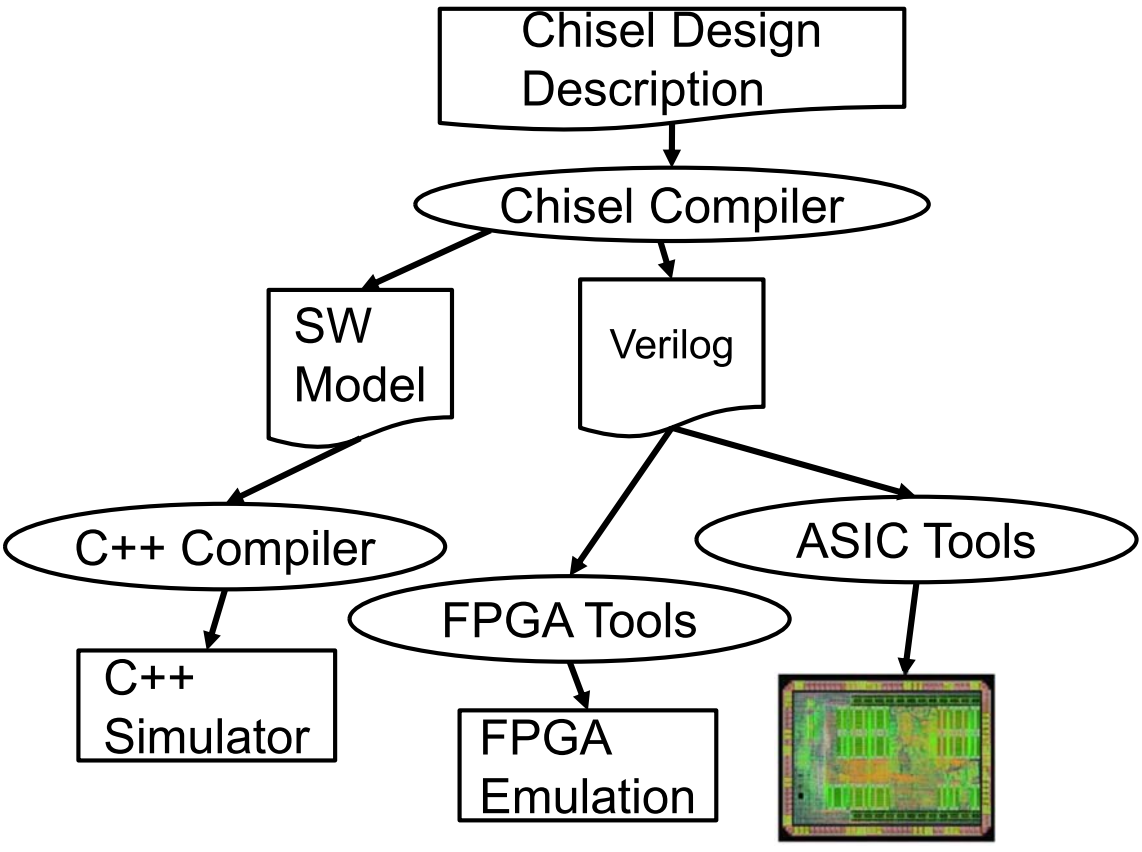
- Rapid growth in the adoption and number of open source software projects
- More than 95% of web servers run Linux variants, approximately 85% of smartphones run Android variants
- Will open source hardware ignite the semiconductor industry? Is RISC-V the hardware industry's Linux?

Why Open Source Hardware?

- **Reducing the cost of development**
  - By creating and sharing open hardware (RISCV, OpenSOC)
- **Closed source IP is a major drag on innovation in all technology spaces**
  - Don't need to be a big company to play – lower barrier of entry
  - Open nature enables customization at *all* levels of the design – not just at the periphery
- **Lower Cost / Complexity for Development**
  - Share hardware AND software stack
    - Compilers, debug, Linux ports
  - Focus NRE and license on new/innovative IP blocks
  - Stop squeezing license costs out of items that students can implement in a summer (license *hard* stuff instead)

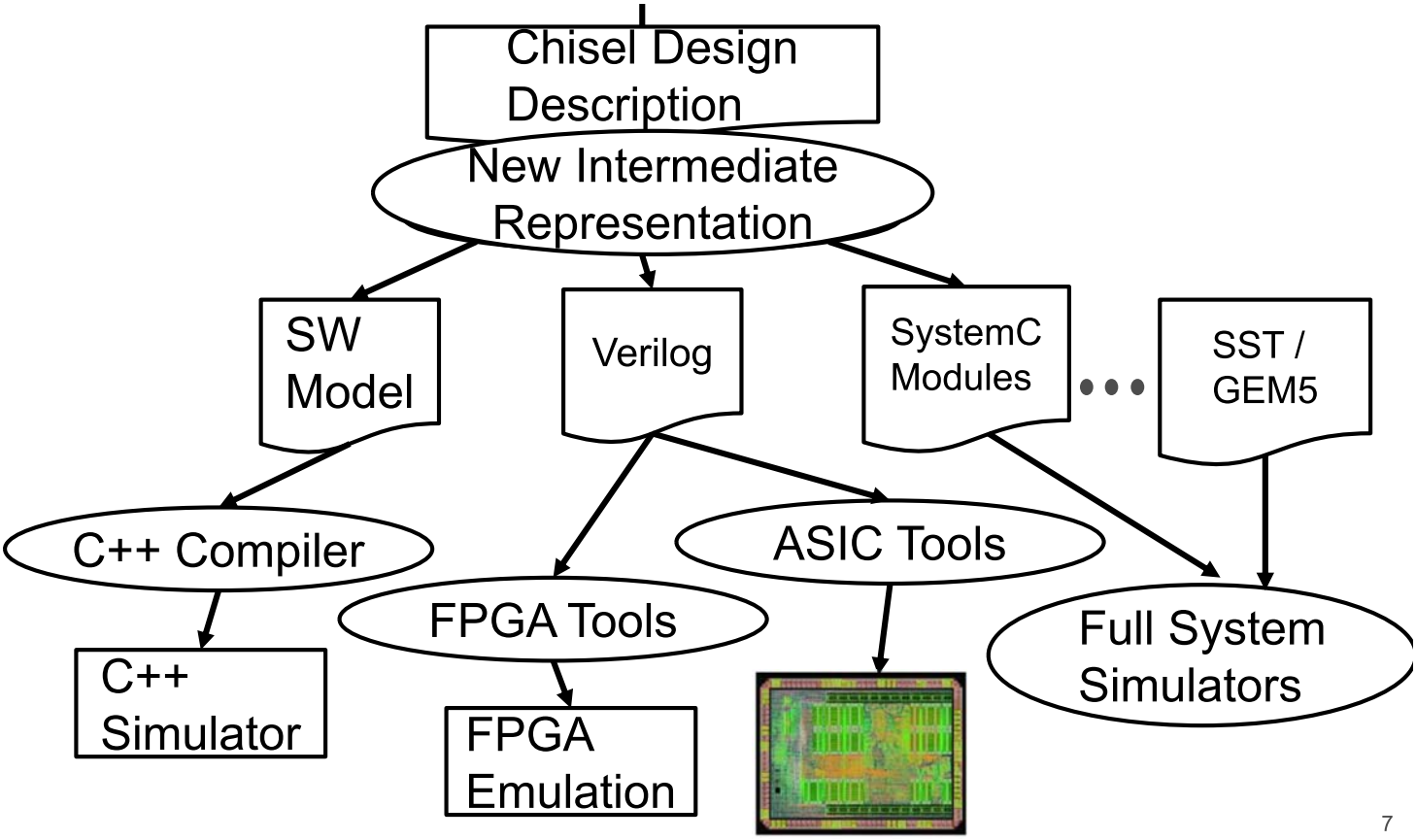
Chisel: A DSL for Hardware Design

Hardware Generation Infrastructure with Integrated Simulation



Chisel: A DSL for Hardware Design

Hardware Generation Infrastructure with Integrated Simulation



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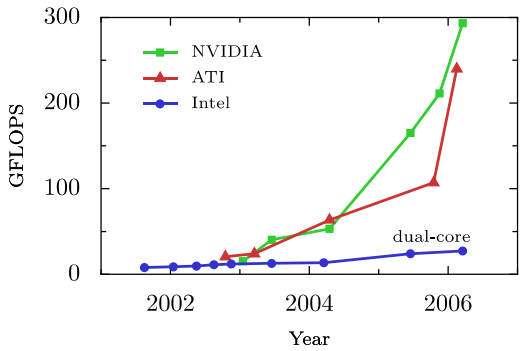
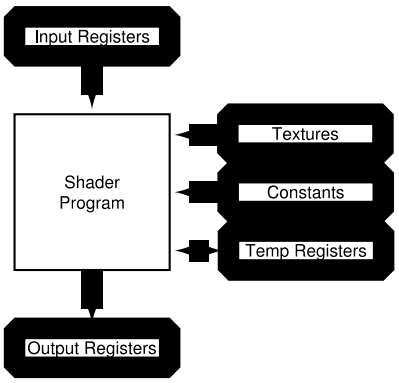
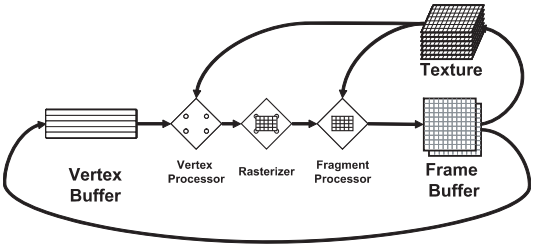
Programmability

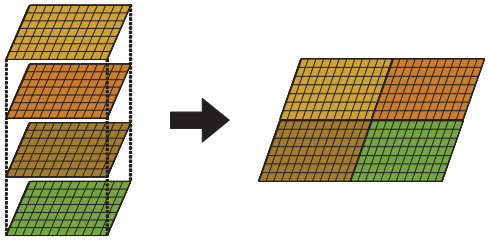
Remember 2004?






```
typedef    OctreeGpu<vec3f, vec4ub> OctreeType;   // 3D float addresses, RGBA values
OctreeType octree( vec3i(2048, 2048, 2048) );    // effective size 2048^3
```

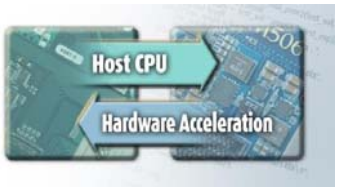




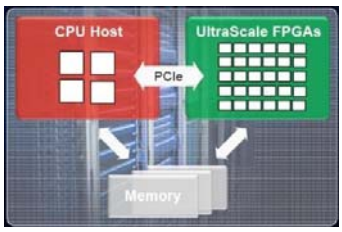
Buck, Owens, Riffel, Lefhon , et al.

Programmability

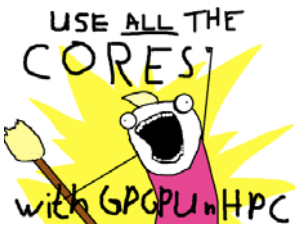
FPGA ecosystem promoting development of new tools and abstractions to accelerate development



- **Parallels with early days of GPGPU computing**
- **New languages raising abstraction levels**
  - OpenCL
  - OpenACC
- **But the tools are still terrible**



ASPIRE

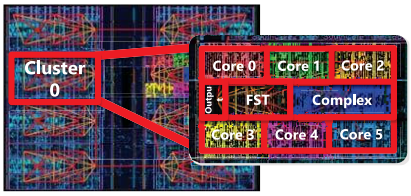


Altera® SDK for OpenCL™

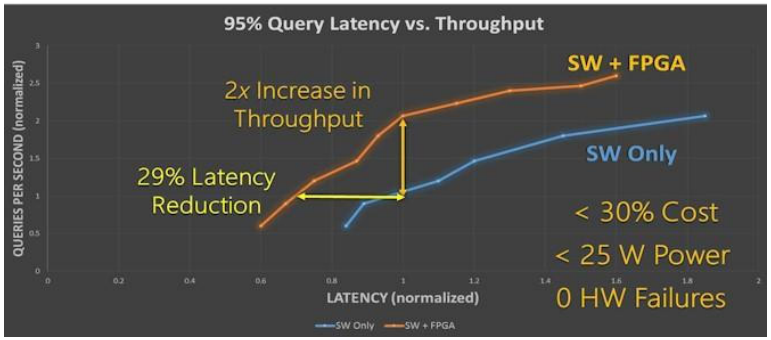
XILINX
ALL PROGRAMMABLE

What's Next?

- **Need to continue to deliver increased performance scaling**
- **FPGAs emerging as the next computational element**
- **Can we get some better tools?**
  - HW design getting better, but not enough
- **Already being deployed at scale**
  - Catapult



1,632 Servers with FPGAs Running Bing Page Ranking Service (~30,000 lines of C++)



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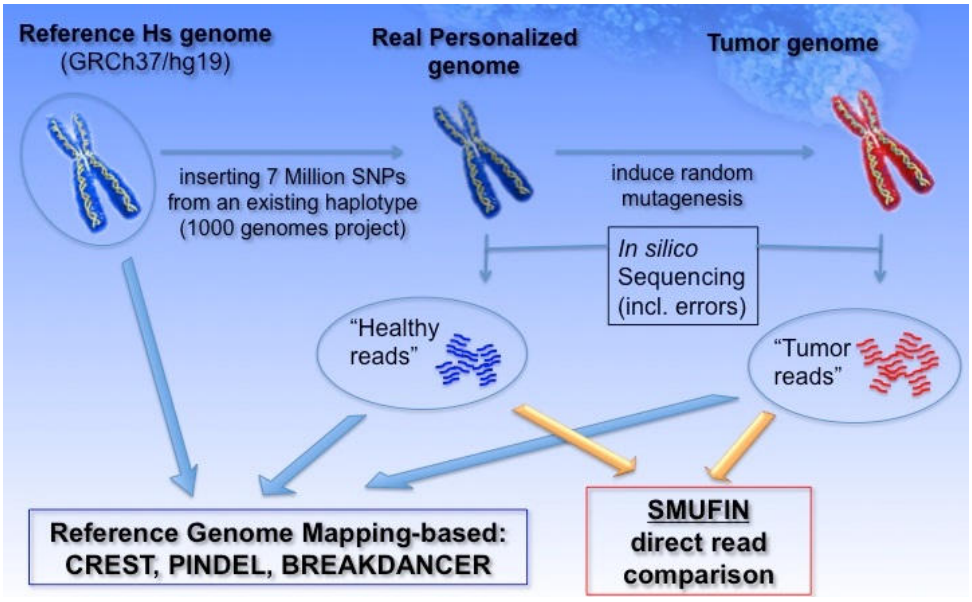
Scaling Genomics Workloads

Jordà Polo <jorda.polo@bsc.es>

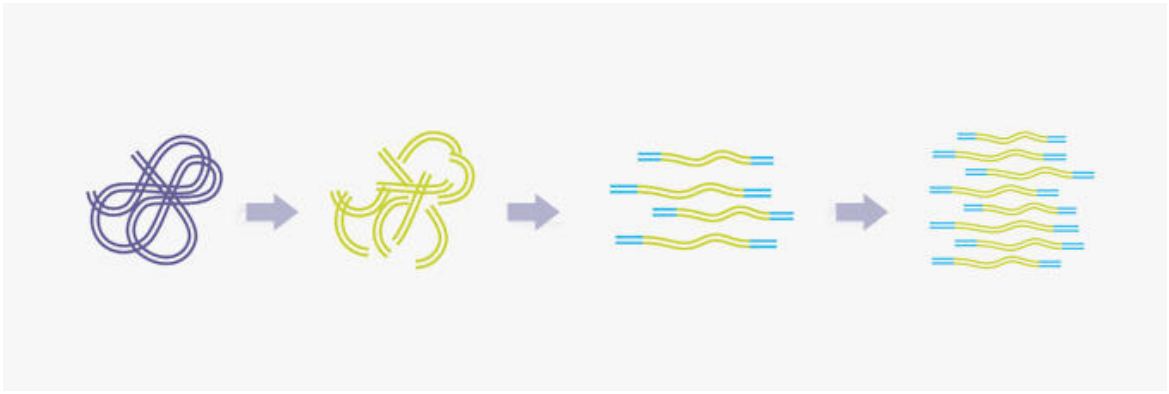
November 17, 2016

SMUFIN

Somatic MUtation FINder: identification and analysis of somatic mutations related to different diseases.



Sequencing and Input Data



TGTTCACACTTGTTTTGTCATTTAAGACATGGTCTTTTCTGGAGAATGTTCCATATGA

x 1,000s of millions

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SMUFIN Redesign

- Original version based on suffix-trees
  - Performance and scalability issues
- Hardware-software co-design
- Reconfigurable from the ground up
- Service-like architecture
- Malleable & scaleable pipeline

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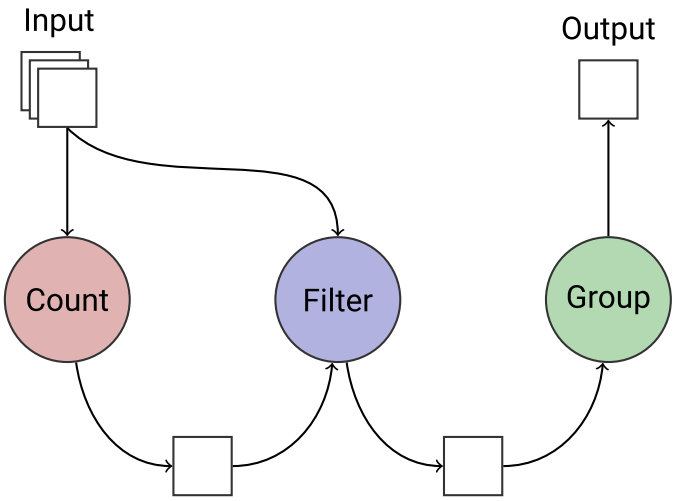
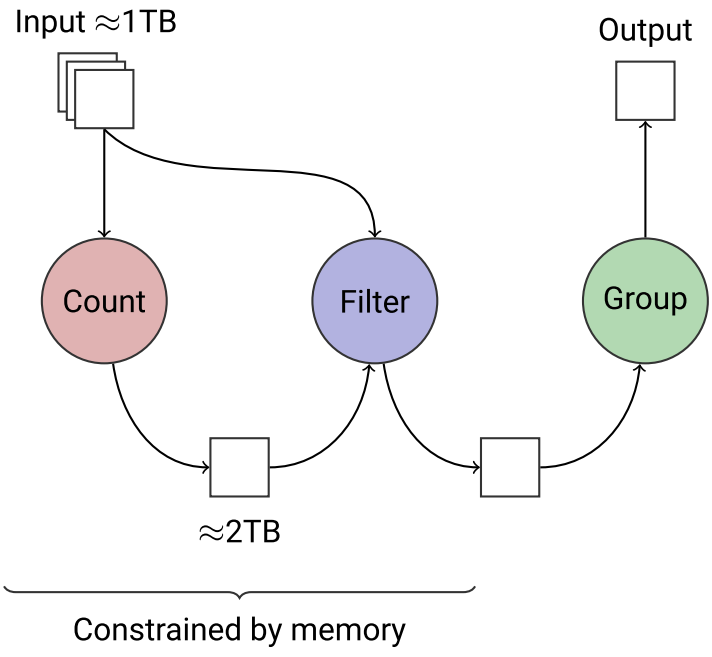
SMUFIN Architecture



SMUFIN Architecture



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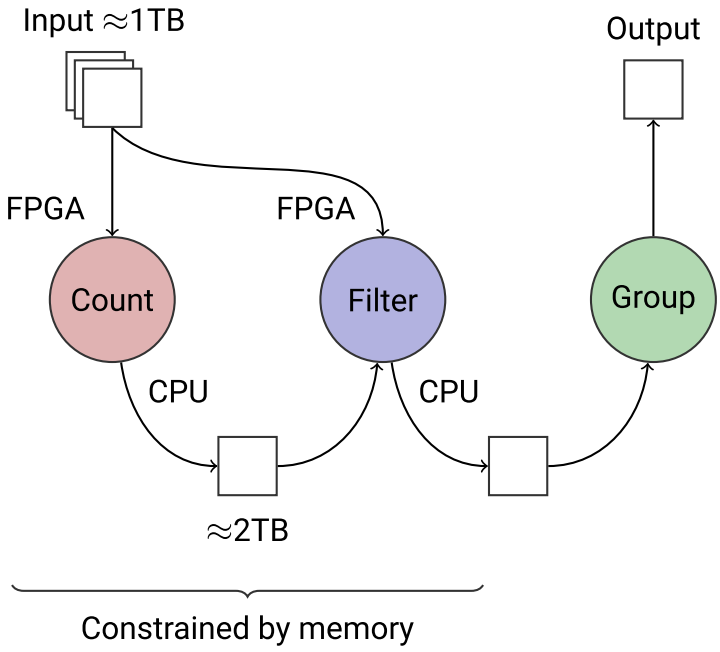

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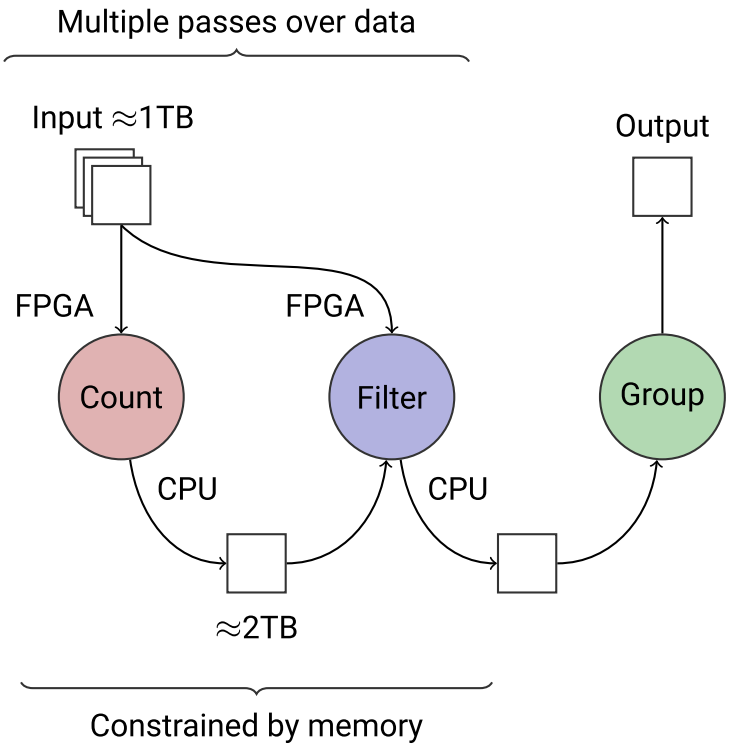

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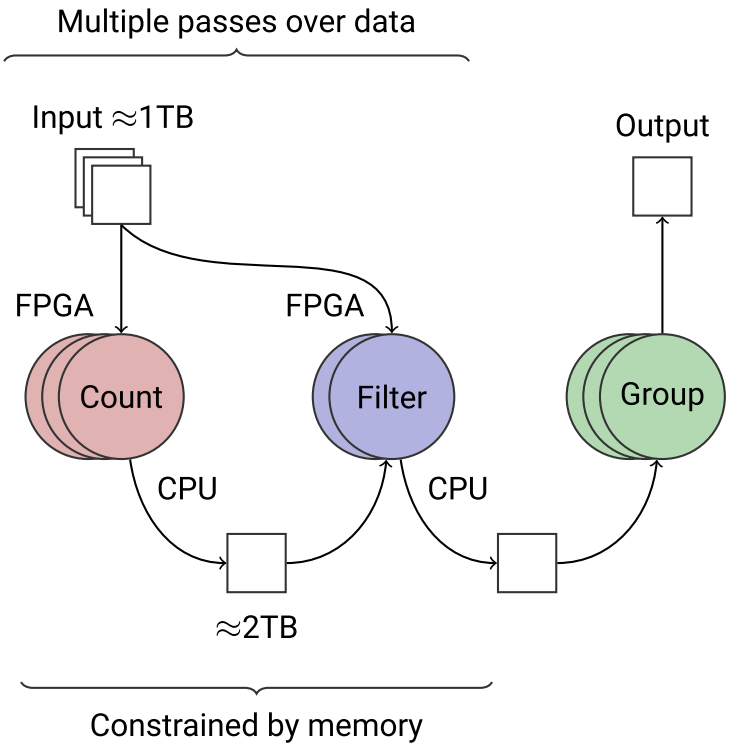
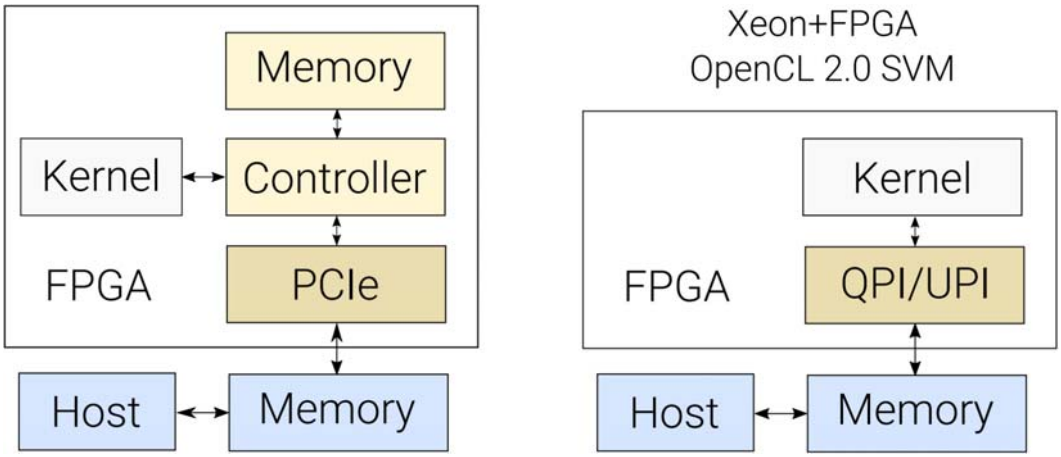


Data Reduction and Amplification

TGTTCACACTTG	TGTTCACACTTG	TGTTCACA	32331010
9C;=;=<9@486	9C;=;=<9@486	GTTCACAC	23310101
		TTCACACT	33101013
AGACATGGTCTT	~~AGACATGGTCTT~~	TCACACTT	31010133
8>9:67AA<9>6	~~8>9:67AA<9>6~~	CACACTTG	10101332

1x **Input** → 0.9x **Quality** → 20x **Split** → 5x **Encode**

Exploring New Models



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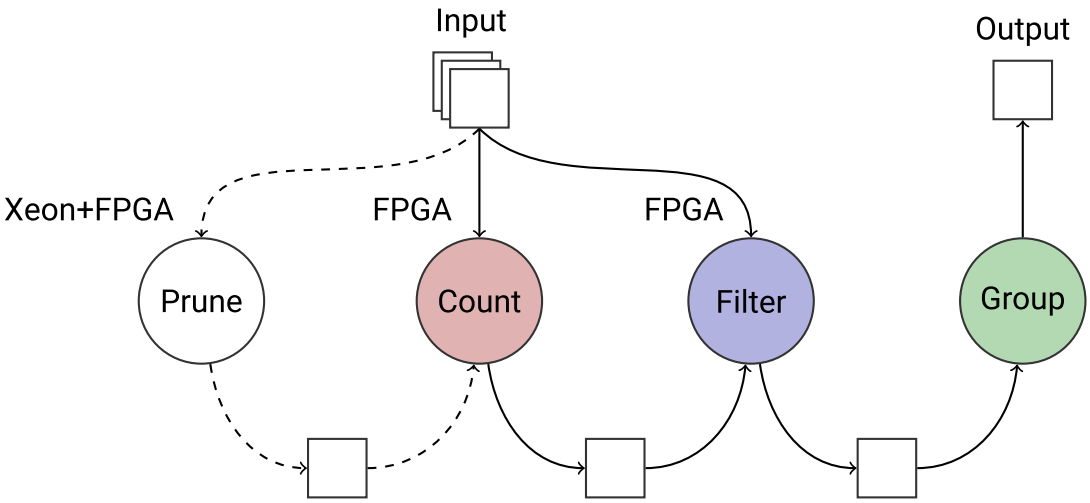

Booth #2511

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